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Application No.: 10/826,805

Docket No.: JCLA12240

<u>REMARKS</u>

Present Status of the Application

The Office Action rejected claims 1-25. Specifically, the Office Action rejected claims 10

and 21 under 35 U.S.C. 112, second paragraph. The Office Action rejected claims 1, 3-9, 12,

14-20 and 23 under 35 U.S.C. 103(a) as being unpatentable over Murata (U. S. Patent 6,483,184)

in view of Durocher et al. (U. S. Patent 6,614,103, hereinafter Durocher). The Office Action

rejected claims 2, 10-11, 13 and 21-22 under 35 U.S.C. 103 (a) as being unpatentable over

Murata and Durocher and in view of Applicant Admitted prior art (AAPA). Applicants have

amended independent claims 1 and 12 to respectively recite the features in previously added

claims 24-25, which are now cancelled. Amendments do not raise new issues. Applicants

have also amended claims 3 and 14 to improve clarity. After entry of the foregoing

amendments, claims 1-25 remain pending in the present application, and reconsideration of those

claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1, 3-9, 12, 14-20 and 23 under 35 U.S.C. 103(a) as being

unpatentable over Murata in view of Durocher. The Office Action rejected claims 2, 10-11, 13

and 21-22 under 35 U.S.C. 103 (a) as being unpatentable over Murata and Durocher and in view

of AAPA. Applicants respectfully traverse the rejections for at least the reasons set forth below.

Applicants have amended independent claims 1 and 12 to respectively recite the features in

previously added claims 24-25, which are now cancelled. The amendments do not raise new

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issue.

terminals.

The Office Action in "Response to Argument" of the Office Action has stated that (first issue) the independent claims 1 and 12 do not recite I/O terminal, and (second issue) the elements 20, 26 and 28 are used as a specific I/O terminal of a chip, and plurality of chips are connected together, then elements 20, 26 and 28 are also used by other chips or other I/O

Applicants respectfully disagree.

1. About the first issue of the I/O terminals, the first patterned conductive film and the second patterned conductive film are respectively connected to the two electrodes of the LED, so that the first patterned conductive film and the second patterned conductive film serve as the two electrode terminals (or usually known as two power terminals) for the LED. Independent claims 1 and 12 have clearly recited these features but not called the I/O terminals. Actually, these power terminals of the LED device are not equal to the I/O terminals of an IC chip. That's why Murata does not equally disclose the present invention.

2. About the second issue for multiple LED's, as for example shown in FIG 2B or FIG 6, one patterned conductive film can be connected with multiple LED's at the corresponding one power electrode for each LED.

In re Murata, as shown in FIGs. 1A-2C, the circuit chip is not the LED device, but is an IC chip. Each of the IC chips has its own set of I/O terminals (also see FIGs. 3A-3B). As shown in FIG 2B, each chip has its own elements 20, 28 and 26 without sharing with the elements 20, 28 and 26 of the other chip. Murata does not disclose mounting two chips commonly using the same elements 20, 28 and 26. The IC chip has several I/O terminals. Bur

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the LED only has two power electrodes, of which on is at operation voltage and one is at ground

voltage as known by the ordinary skilled artisans. Therefore, IC chip is not equal to LED chip.

And, Murata doe not disclose the same coupling structure.

The Office Action states "if elements 20, 28 and 26 are used by a specific I/O terminal of a

chip, and plurality of chips are connected together, then elements 20 are also used by other chips

or other I/O terminals (Emphasis added)". However, Murata does not disclose this way. As

mentioned above, each chips has its own elements 20, 28 and 26, which commonly used by the

other chip. Applicants respectfully remind that "hindsight" or "personal knowledge" should not

be involved.

Also and, Murata is directed to packaging the IC chips, but not the LED device. Basically,

Murata is nonanalogous to the present invention. Also and, Applicants respectfully reminds

that "hindsight" and "improperly construing on prior art disclosure" should be avoided.

3. In re Durocher, the LED package is disclosed. However, Durocher discloses a different

package structure to the present invention. Also and, Murata is nonanalogous to the LED

package and cannot be directly modified by the disclosure from Durocher. Durocher does not

specifically provide the motivation to modify Murata either.

4. AAPA does not disclose the missing features in Murata and Durocher, with respect to

amended independent claims 1 and 12.

5. With respect to claims 3 and 14, as shown in FIG. 7A, now, at least one of m and n is

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greater than or equal to 2. Therefore, m and n are not equal to 1. Amendments, as previously discussed about multiple LED chips, do not raise new issue. Claims 3 and 14 now is further define over the prior art.

For at least the foregoing reasons, Applicants respectfully submit that independent claims 1 and 12 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-11 and 13-25 patently define over the prior art references as well, wherein claims 3-9, 14-20, and 24-25 further define over the prior art references. Claims 3 and 14 further define over the prior art references.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-23 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted, J.C. PATENTS

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